REMARKS

1. The application was filed with 23 claims. Claims 1-14 and 17-19 are pending in the application. Claims 15 and 16 have been cancelled. The Examiner is thanked for withdrawing her rejections under 35 U.S.C. § 102(b) and § 102(e). The Examiner is also thanked for allowing Claims 7-14 and 17-19, and Claims 5-6 if they are amended to incorporate all the limitations of the base claim and any intervening claims.

2. The undersigned and Examiner Cox conducted a brief interview on January 30, 2004, concerning the allowability of Claims 1-4. The undersigned pointed out that the reference did not disclose the outputs of the amplifier claimed in Claims 1-4 and that the reference did not teach a delay circuit, or that a plurality of the delay units could be placed in series to generate a longer delay time. The Examiner did not agree, and agreement was not reached with respect to Claims 1-4. The Examiner is thanked for her courtesy in granting the interview.

3. The Examiner has rejected Claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,414,556 to Masayuki Mizuno ("Mizuno"). The rejection states that Fig. 4 of Mizuno substantially discloses the circuit described by Claim 1 of the present application, as well as Claims 2 and 3. While the rejection includes Claim 4, no rejection is articulated with respect to Claim 4. The rejection further admits that Mizuno does not disclose a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals. Office Action, p. 3, lines 1-3. The Office Action also states that the circuit of Mizuno will "inherently generate a delay." Office Action, p. 5, "Response to Arguments," lines 6-8.

The rejection further states that it is well known to one skilled in the art that circuits may have multiple output taps dependent on the desired outcome and the particular environment. It would have been obvious to one skilled in the art that the drain of MP_{35} could be tapped as an output of the circuit, in addition to the output of MP_{36}. Office Action, p. 3, lines 3-6. It would be obvious, states the rejection, because

the signal from the drain of MP_{35} could be used to output a low level signal that is opposite of the signal being generated from MP_{36}.

Applicants traverse the rejection. Independent Claims 1 and 4 are specifically directed to a delay unit, while Mizuno is not directed to a delay unit, but to a level converter. Fig. 4 does not describe or suggest a delay unit, but a six-transistor level converter, which is also depicted in Figs. 6 and 8 of Mizuno. In addition, as admitted in the Office Action, the voltage converter of Fig. 4 does not have "a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals," as claimed in Claim 1 and Claim 4.

A reference may be used for all that it fairly teaches or suggests to one having skill in the art, but when a reference is silent about an asserted inherent characteristic, it must be clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *Continental Can Co. v. Monsanto Co.*, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991). The circuit of Fig. 4 of Mizuno is described in the reference as a "level converter." The reference does not state that the level converter may be used as a delay unit, and indeed, the reference teaches other circuits, a series of inverters as shown in Figs. 3 and 12, for this function. Since any circuit will require time for an electronic signal to pass through the circuit, one could make the same argument for any circuit, i.e., that any circuit would "inherently generate a delay."

Claims 1 and 4, and their dependent claims, claim a four-transistor delay unit whose advantage is to use the all the voltage "headroom" available from a power supply. The reference is a six-transistor level converter, with different inputs, different outputs, and different internal connections, used for a different purpose, shifting or limiting a voltage level. The reference does not describe or suggest all the limitations of the inventions claimed in Claims 1-4.

Nevertheless, Applicant has amended Claims 1 and 4 in a non-narrowing manner to recite a functional limitation that the delay period in the delay unit is determined by the input control and supply voltage. The amendment is non-narrowing because there are only two voltage inputs to the unit, the input signal and the control input and supply voltage. If the delay unit may be varied independently of the input

signal, only the control input and supply voltage remains, and thus the amendment is non-narrowing. No new matter was added in amending the claims, for which support is found at least in the specification, p. 5, in the paragraph from lines 15-25. The Examiner is respectfully requested to withdraw the rejections of Claims 1-4 under 35 U.S.C. § 103(a).

The undersigned has also amended Claims 2, 3, 5, and 6 in order to better define the inventions claimed in independent Claims 1 and 4. No new matter has been added in amending the claims. Support for the amended Claims is found at least in the specification, on p. 6, lines 10-22, and Figs. 3b and 14.

4. Applicant again thanks the Examiner for withdrawing previous rejections under 35 U.S.C. § 102(b) and § 102(e), and for allowing a number of the claims. Claims 1 and 4 have been amended in a non-narrowing manner, and Claims 2, 3, 5, and 6 have also been amended to better define the invention. Applicant respectfully requests the Examiner to withdraw the rejections and to advance the Application to allowance.

Respectfully submitted,

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